

REMARKS

Claims 4-15 were pending and rejected. Claims 4-5 and 8-14 are amended, and claims 6-7 are cancelled, without prejudice to pursue the original claims in a related application. Claim 16 is new. Thus, after entry of this amendment, claims 4-5 and 8-16 are currently pending. No new matter has been added.

Claim Objections

In the Action, claim 11 was objected to for informalities. In response, this claim has been amended to overcome the objections. Thus, reconsideration of this claim, as amended, is respectfully requested with express withdrawal of the objections.

Claim Rejections under 35 USC §112

In the Action, claims 11-15 were rejected under 35 USC §112, first paragraph, for failing to comply with the written description and enablement requirements. In response, these claims have been amended to overcome the rejections. Thus, reconsideration of these claims, as amended, is respectfully requested with express withdrawal of the rejections.

Claim Rejections under 35 USC §103

Claims 4, 6, and 8 were rejected under 35 USC §103(a) as unpatentable over Choo (US 2001-0049154) in view of Kameshima (US 2002-0196898).

Claim 5 was rejected under 35 USC §103(a) as unpatentable over Choo in view of Kameshima and Jeon (US 2002-0149318).

Claims 7, 9, and 10 were rejected under 35 USC §103(a) as unpatentable over Choo in view of Kameshima and Jeromin (US 6,075,248).

In response, Applicant asserts that these references, alone or in any combination, fail to disclose or even suggest each and every limitation of the present claims.

For example, present independent claim 4, as amended, recites the following limitations (*emphasis added*):

a substrate including a gate driver region, a data pad region, and a storage capacitor region;
a first conductive line formed in the data pad region;

a second conductive line formed in the storage capacitor region, a portion of the second conductive line functioning as a capacitor electrode of a storage capacitor;

a first switching element formed in a pixel region;

a first transparent layer including first and second transparent electrodes formed on the first and second conductive lines, respectively;

an insulating layer having a first contact hole extending to the first transparent electrode on the first conductive line in the data pad region and a second contact hole extending to a drain electrode of the first switching element in the pixel region;

an organic layer formed on the insulating layer, the organic layer having a first removed portion exposing the first transparent electrode in the data pad region and a second removed portion exposing the drain electrode of the first switching element in the pixel region; and

a second transparent layer formed on the organic layer, the second transparent layer including a third transparent electrode directly connected to the first transparent electrode through the first contact hole in the data pad region and a fourth transparent electrode directly connected to the drain electrode through the second contact hole in the pixel region,

wherein a portion of the organic layer in the storage capacitor region is removed, and the fourth transparent electrode extends to the storage capacitor region to be disposed directly on the insulating layer in the storage capacitor region, thereby forming the storage capacitor comprising the capacitor electrode, the second transparent electrode, a portion of the insulating layer in the storage capacitor region, and the fourth transparent electrode extending to the storage capacitor region.

In reference to Figs. 5C-5F, Choo discloses a second storage electrode 60 or 160 formed on a protection layer 181 and a second insulation layer 183 formed on the second storage electrode 60 or 160 and the protection layer 181. Choo further discloses a contact hole 195 formed to expose the second storage electrode 60 or 160 and a pixel electrode 62 or 211 formed on the second insulation layer 183 to be connected to the second storage electrode 60 or 160 through the contact hole 195.

Accordingly, Choo explicitly discloses an additional process for forming the second storage electrode 60 or 160 along with a necessary process for forming the pixel electrode 211. Clearly, Choo expressly teaches increasing the number of processes, which is different than the subject matter of the present claims.

Moreover, the second storage electrode 60 or 160 of Choo functions as an electrode of a storage capacitor, and the pixel electrode 62 or 211 does not function as an electrode of

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the storage capacitor. According to Choo, the pixel electrode 62 or 211 merely electrically connects the second storage electrode 60 or 160 to a drain electrode, which is different than the subject matter of the present claims.

In sharp contrast, present independent claim 4, as amended, recites, “wherein a portion of the organic layer in the storage capacitor region is removed, and the fourth transparent electrode extends to the storage capacitor region to be disposed directly on the insulating layer in the storage capacitor region, thereby forming the storage capacitor comprising the capacitor electrode, the second transparent electrode, a portion of the insulating layer in the storage capacitor region, and the fourth transparent electrode extending to the storage capacitor region.” Support for these limitations may be found throughout Applicants’ specification, e.g., Figs. 5-14 and pars. 39-61.

In one aspect, referring to Figs. 5-14, a portion of the organic layer 250 in the storage capacitor region is removed, and the fourth transparent electrode (i.e., the pixel electrode directly connected to the drain electrode 225) extends to the storage capacitor region to be disposed directly on the insulating layer 240 in the storage capacitor region, thereby forming the storage capacitor comprising the capacitor electrode 226, the second transparent electrode 231, the portion of the insulating layer 240 in the storage capacitor region, and the fourth transparent electrode extending to the storage capacitor region. Accordingly, the fourth transparent electrode functions as a storage electrode of the storage capacitor.

Moreover, the ancillary Kameshima, Jeon, and Jeromin references fail to remedy the deficiencies of the cited Choo reference. For example, Kameshima is merely relied on for purportedly disclosing scanning and/or data processing integrated circuitry located at ends of gate and data lines. In another example, Jeon is merely relied on for purportedly disclosing a scanning circuit including a shift register. In another example, Jeromin is merely relied on for purportedly disclosing extending an electrode over a FET and providing shielding electrodes for circuitry.

Therefore, since the cited Choo reference fails to disclose or even suggest each and every limitation of present independent claim 4, and the ancillary references fail to remedy the deficiencies of Choo, present independent claim 4, as amended, and any claims

dependent thereon are considered to be in condition for allowance, and such allowance is respectively requested.

Present independent claim 11 has been amended in a manner similar as present independent claim 4. Therefore, present independent claim 11, as amended, including any claims respectively dependent thereon are considered to be in condition for allowance for at least the same reasons as discussed above in reference to present independent claim 4, and such allowance is respectively requested.

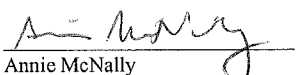
New Claims

Claim 16 is new and is considered to be in condition for allowance for at least its dependence on present claim 1, and such allowance is respectively requested.

CONCLUSION

For the foregoing reasons, Applicants respectfully submit that the pending claims are in condition for allowance. Reconsideration and withdrawal of the rejections are respectfully requested and a timely Notice of Allowance is solicited.

If there are any questions regarding any aspect of the application, please call the undersigned at (949) 752-7040.

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<u>Electronically Filed by:</u>	
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Respectfully submitted,



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